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SIMULATION AND HARDWARE IMPLEMENTATION OF INTERLEAVED TECHNIQUE BASED DC-DC BUCK-BOOST CONVERTER

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ABSTRACT

DC-DC converters has wide range of applications in renewable energy systems, hybrid systems, electric vehicles, fuel cells, and industries. Interleaved topology of dc-dc converter has capabilities of correcting power factor, decreasing input/output ripples, and increasing efficiency, and its specifications of capacitors and inductors are reasonable with low voltage and current stress on switches and diodes. This paper presents MATLAB simulation and hardware model of dc- dc buck-boost converter based on interleaved technique. With a desired output prototype of 36V,4.16A and 150W from a fluctuating input supply of 26 to 43V, two interleaved buck and two interleaved boost converter are arranged in cascade connection with a damping circuit. Various specifications of components are derive dusing steady-state analysis and triggering pulses for MOSFETs are generate dusing PIC micro controller.

KEYWORDS: interleaved, buck-boost, dc-dc converter, MATLAB/Simulink.

INTRODUCTION

DC-DC converter has a number of applications, due to which it has regular inputs from researchers. Applications include solar energy systems, wind energy systems, fuel cell, Hybrid Electric Vehicles(HEV) and Electric Vehicle (EV) ,fuel cell, communication systems, Maximum Power Point Tracking (MPPT) and many more.DC-DC converters has many topologies such as buck, boost, buck-boost, CUK, SEPIC, Multi-Input Multi-Output (MIMO),fly back, interleaved, etc. DC-DC converters can be categorized into inverting or non-inverting isolated or non-isolated, and Zero Voltage Source(ZVS) or Zero Current Source(ZCS) [1-5].
Interconnection of DC-DC converters in an alternative pattern is known as interleaved technique based topology. Interleaved technique based DC-DC converters have more efficiency with less input/output ripple. Hence, this increases dynamics and power handling capability of the dc-dc converter with components of smaller size and less power ratings. Depending on the various practical applications, these converter can be buck, boost, or buck-boost,and inverting or non-inverter [6-7].

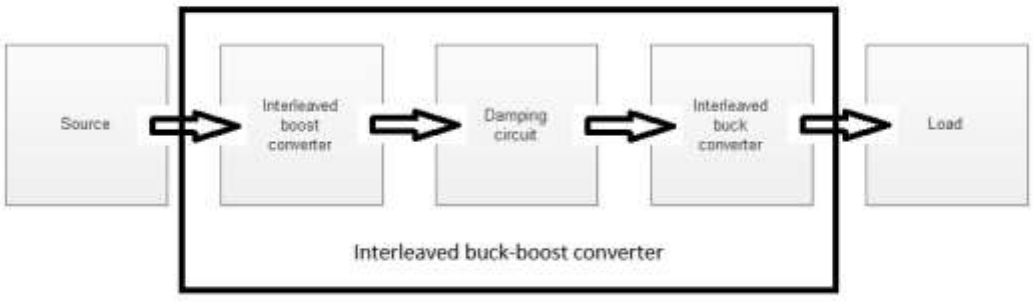

Figure1 Block diagram of proposed converter

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Figure1 shows block diagram of the proposed converter. It contains two boost converters arranged in interleaved pattern along with two buck converters arranged in interleaved pattern ,to decrease voltage and current stress on switches. These two blocks are connected in cascade combination with damping circuit to increase dynamics of the system, and reduce input/output voltage and current ripples [8-11]

Figure2 shows the circuit diagram of the proposed converter. Two inductors of interleaved boost converter and two inductors of buck converter forms coupled inductor due to the occurrence of mutual inductance, there by reducing the inductors sizes [12]. Cascade combination of the set wo inter leaved boost and buck converter make it a buck-boost converter. This cascade combination are connected with a damping circuit in between the circuit to increase the dynamics of the converter [13].

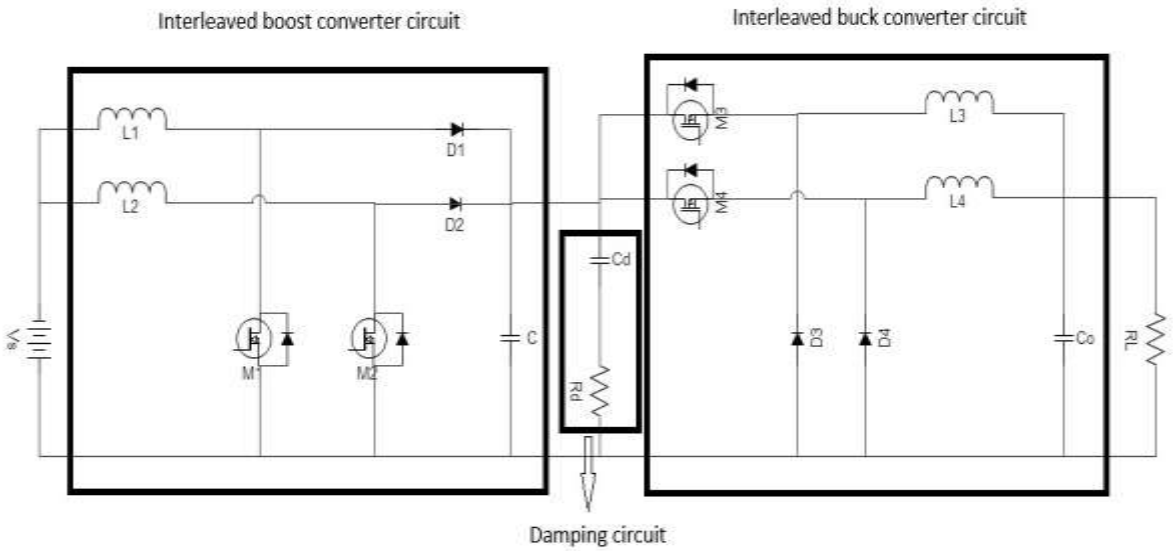

Figure 2 Circuit diagram of proposed converter

C and C_0 are the boost and buck stage filter capacitors respectively; hence converter has low ripple DC voltage. Four switches divide voltage and current stress among themselves due to which stability of the converter increases and power losses are reduced

OPERATING PRINCIPLE

Inter leaved buck-boost DC-DC converter is operated in Continuous Conduction Mode (CCM) in six different modes of operation .Four MOSFETs are used in the circuit, and has feasible controller circuit to generate PWM by using bread board .In boost mode, switches of interleaved boost converter i.e. M3 and M4 are completely turned ON, where as switches of inter leaved buck converter i.e .M1 and M2 are operated with PWM. Figure 3 shows the circuit and switching frequency of converter while operating in boost mode

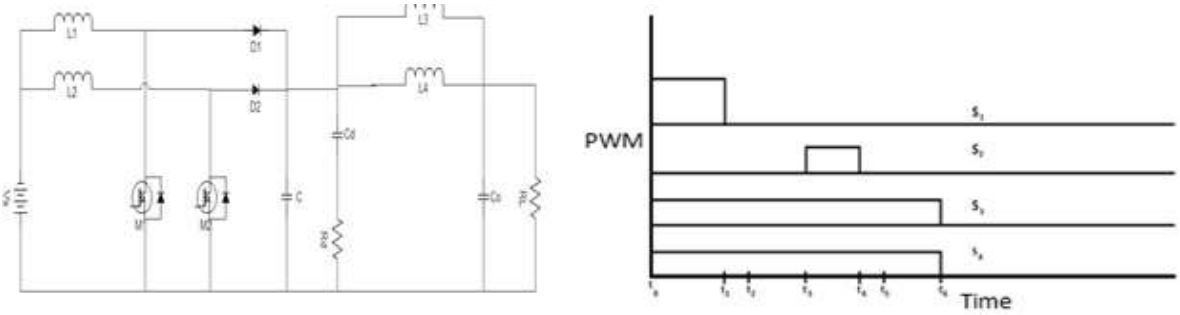

Figure 3 Circuit and switching frequency boost mode operation of converter

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In buck mode, switches of inter leaved boost converter i.e .M3 and M4 are operated with PWM, where as switches of inter leaved buck converter i.e. M1 and M2 are completely turned OFF. Figure 4 a shows the circuit and switching frequency of the converter operating in buck mode

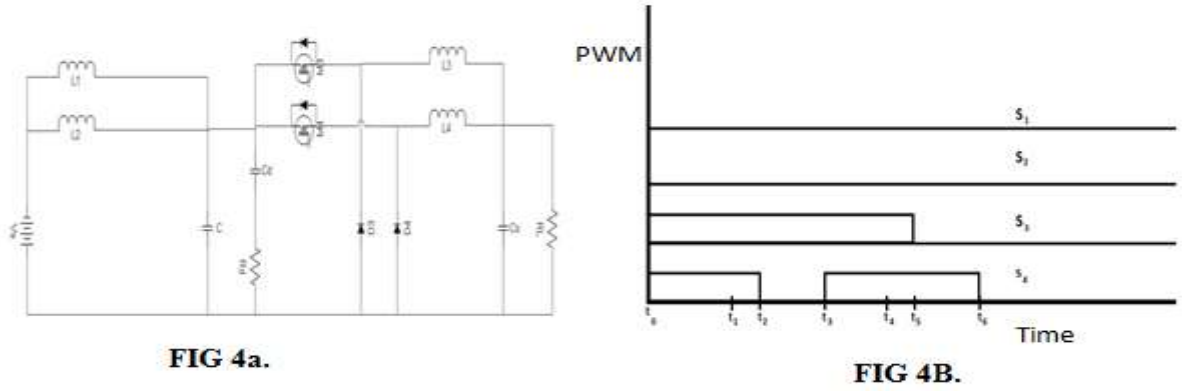

FIG 4a.

FIG 4B.

Figure 4a Circuit of buck mod eoperation of the converter
Figure 4b Switching frequency of buck mode operation of the converter

OPERATING MODES

The proposed converter is operated in six different modes to derive expressions for finding parameters of the components.Figure5 shows the block diagram of operating DC-DC converter. Table1 shows time period for six modes of operation. According to the type of application, changes in duty ratio of MOSFETs can be derived easily[14]. Different modes of operations discussed in various literatures [15-16] have been depicted in Figures 6(a) to 6(f).

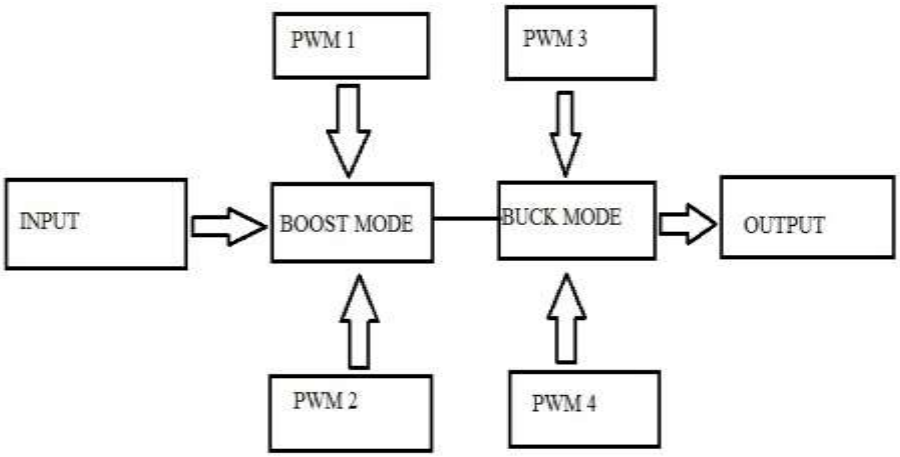

Figure 5 Block diagram of DC-DC converter operation.

Table1 Time period for six modes of operation

INTERVAL	TIME
t_0-$t_1$andt_3-t_4	$d_1$or$_2$.T
t_1-$t_2$andt_4-t_5	($d_3$or$_4$-$d_1$or$_2$-0.5).T
t_2-$t_3$andt_5-t_6	(1-$d_3$or$_4$).T

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MODE 1

IntervalT0-T1: M1, M3, and M4 a returned ON, where as M2 is turned OFF. Hence, inductor L1 stores energy and inductor L2 transfers energy. Figure 6(a) shows equivalent circuit for mode1. Voltage across inductors and current through capacitors are expressed through equations (1) to (7).

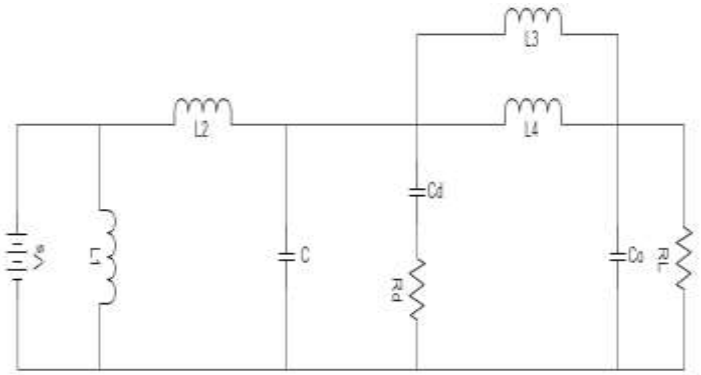

Figure 6(a) Equivalent circuit for Mode 1

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_s \tag{1}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = v_s - v_{C_1} \tag{2}$$

$$v_{L_3} = L_3 \frac{di_{L_3}}{dt} = v_{C_1} - v_{out} \tag{3}$$

$$v_{L_4} = L_4 \frac{di_{L_4}}{dt} = v_{C_1} - v_{out} \tag{4}$$

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} = i_{L_2} - (i_{L_3} + i_{L_4}) - \frac{v_{C_1} - v_{C_d}}{R_d} \tag{5}$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt} = (i_{L_3} + i_{L_4}) - \frac{v_{out}}{R_L} \tag{6}$$

$$i_{C_d} = C_d \frac{dv_{C_d}}{dt} = \frac{v_{C_1} - v_{C_d}}{R_d} \tag{7}$$

MODE 2

IntervalT1-T2: M1 and M2 are turned ON, where as M3 and M4 are turned OFF. Hence, inductor L1 and inductor L2 Transfers energy. Figure 6(b) shows equivalent circuit for mode2. Voltage across inductors and current through capacitors are expressed through equations (8) to (14).

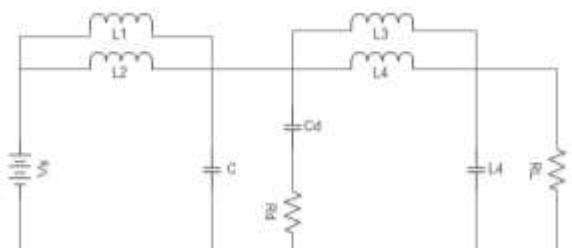

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Figure 6(b) Equivalent circuit for Mode 2

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_s - v_{C_1} \tag{8}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = v_s - v_{C_1} \tag{9}$$

$$v_{L_3} = L_3 \frac{di_{L_3}}{dt} = v_{C_1} - v_{out} \tag{10}$$

$$v_{L_4} = L_4 \frac{di_{L_4}}{dt} = v_{C_1} - v_{out} \tag{11}$$

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} = (i_{L_1} + i_{L_2}) - (i_{L_3} + i_{L_4}) - \frac{v_{C_1} - v_{C_d}}{R_d} \tag{12}$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt} = (i_{L_3} + i_{L_4}) - \frac{v_{out}}{R_L} \tag{13}$$

$$i_{C_d} = C_d \frac{dv_{C_d}}{dt} = \frac{v_{C_1} - v_{C_d}}{R_d} \tag{14}$$

MODE 3

IntervalT2-T3: M3 is turned ON, where as M1, M2, and M4 are turned OFF. Hence ,inductor L3 stores energy and inductor L4 transfers energy. Figure6(c) shows equivalent circuit for mode3.Voltage across inductors and current through capacitors are expressed through equations (15) to (21).

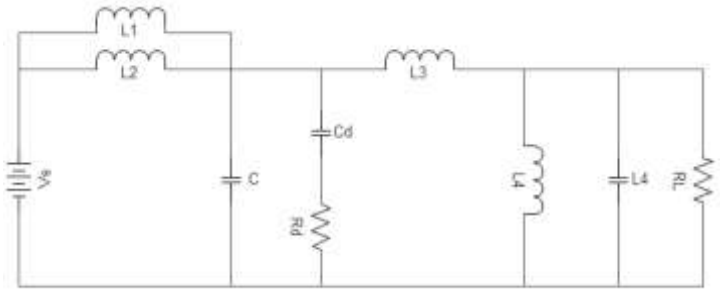

Figure 6(c) Equivalent circuit for Mode 3

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$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_s - v_{C_1} \quad (15)$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = v_s - v_{C_1} \quad (16)$$

$$v_{L_3} = L_3 \frac{di_{L_3}}{dt} = v_{C_1} - v_{out} \quad (17)$$

$$v_{L_4} = L_4 \frac{di_{L_4}}{dt} = v_{out} \quad (18)$$

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} = (i_{L_1} + i_{L_2}) + i_{L_3} - \frac{v_{C_1} - v_{C_d}}{R_d} \quad (19)$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt} = (i_{L_3} + i_{L_4}) - \frac{v_{out}}{R_L} \quad (20)$$

$$i_{C_d} = C_d \frac{dv_{C_d}}{dt} = \frac{v_{C_1} - v_{C_d}}{R_d} \quad (21)$$

MODE 4

IntervalT3-T4: M2, M3, and M4 are turned ON, where as M1 is turned OFF .Hence, inductor L2 stores energy and inductor L1 transfers energy. Figure6(d) shows equivalent circuit for mode 4. Voltage a cross inductors and current through capacitors are expressed through equations (22) to (28).

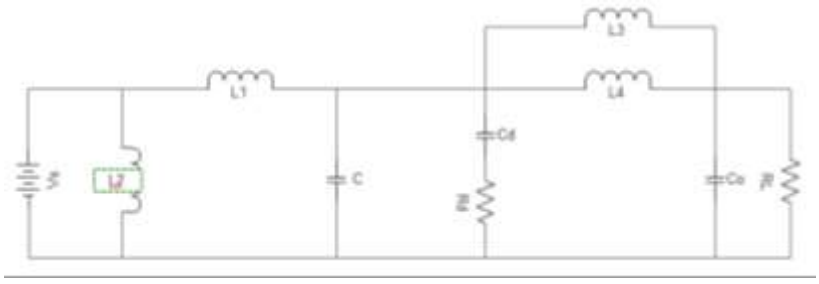

Figure 6(d) Equivalent circuit for Mode 4

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_s - v_{C_1} \quad (22)$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = v_s \quad (23)$$

$$v_{L_3} = L_3 \frac{di_{L_3}}{dt} = v_{C_1} - v_{out} \quad (24)$$

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$$v_{L_4} = L_4 \frac{di_{L_4}}{dt} = v_{C_1} - v_{out} \tag{25}$$

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} = i_{L_1} - (i_{L_3} + i_{L_4}) - \frac{v_{C_1} - v_{C_d}}{R_d} \tag{26}$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt} = (i_{L_3} + i_{L_4}) - \frac{v_{out}}{R_L} \tag{27}$$

$$i_{C_d} = C_d \frac{dv_{C_d}}{dt} = \frac{v_{C_1} - v_{C_d}}{R_d} \tag{28}$$

MODE 5

IntervalT4-T5: M1 and M2 are turned ON, where as M3 and M4 are turned OFF. Hence, inductor L1 stores energy and inductor L2 transfers energy. Figure6(e) shows equivalent circuit for mode5. Voltage across inductors and current through capacitors are expressed through equations (29) to (35).

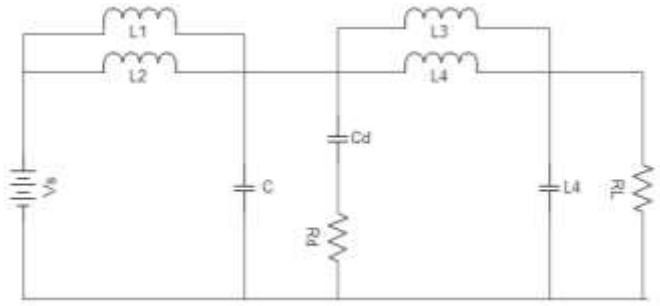

Figure 6(e) Equivalent circuit for Mode 5

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_s - v_{C_1} \tag{29}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = v_s - v_{C_1} \tag{30}$$

$$v_{L_3} = L_3 \frac{di_{L_3}}{dt} = v_{C_1} - v_{out} \tag{31}$$

$$v_{L_4} = L_4 \frac{di_{L_4}}{dt} = v_{C_1} - v_{out} \tag{32}$$

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} = (i_{L_1} + i_{L_2}) - (i_{L_3} + i_{L_4}) - \frac{v_{C_1} - v_{C_d}}{R_d} \tag{33}$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt} = (i_{L_3} + i_{L_4}) - \frac{v_{out}}{R_L} \tag{34}$$

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$$i_{C_d} = C_d \frac{dv_{C_d}}{dt} = \frac{v_{C_1} - v_{C_d}}{R_d} \tag{35}$$

MODE 6

IntervalT5-T6: M4 is turned ON, where as M1, M2, and M3, are turned OFF .Hence, inductor L4 stores energy and inductor L3 transfers energy. Figure6(f) shows equivalent circuit for mode 6. Voltage across inductors and current through capacitors are expressed through equations (36) to (47)

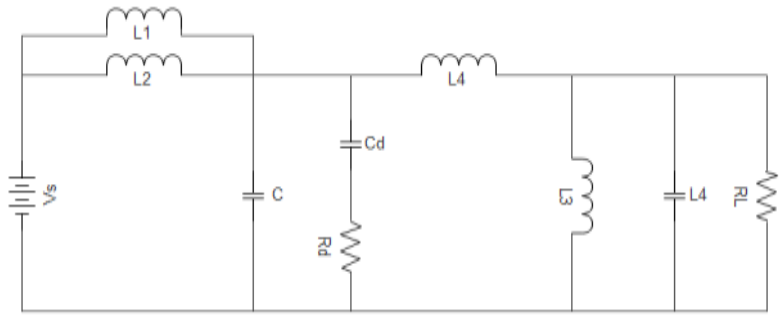

Figure 6(f) Equivalent circuit for Mode 6

$$v_{L_1} = L_1 \frac{di_{L_1}}{dt} = v_s - v_{C_1} \tag{36}$$

$$v_{L_2} = L_2 \frac{di_{L_2}}{dt} = v_s - v_{C_1} \tag{37}$$

$$v_{L_3} = L_3 \frac{di_{L_3}}{dt} = v_{out} \tag{38}$$

$$v_{L_4} = L_4 \frac{di_{L_4}}{dt} = v_{C_1} - v_{out} \tag{39}$$

$$i_{C_1} = C_1 \frac{dv_{C_1}}{dt} = (i_{L_1} + i_{L_2}) - i_{L_4} - \frac{v_{C_1} - v_{C_d}}{R_d} \tag{40}$$

$$i_{C_2} = C_2 \frac{dv_{C_2}}{dt} = (i_{L_3} + i_{L_4}) - \frac{v_{out}}{R_L} \tag{41}$$

$$i_{C_d} = C_d \frac{dv_{C_d}}{dt} = \frac{v_{C_1} - v_{C_d}}{R_d} \tag{42}$$

On applying averaging technique [4] on equations derived from six modes of operations are as follows

$$L_1 \left[\frac{di_{L_1}}{dt}\right]_T = L_2 \left[\frac{di_{L_2}}{dt}\right]_T = V_s - V_{C1}(1 - d_{1or2}) \tag{43}$$

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$$L_3\left[\frac{di_{L_3}}{dt}\right]_T = L_4\left[\frac{di_{L_4}}{dt}\right]_T = -V_{out} + V_{C1}d_{3or4} \tag{44}$$

$$C_1\left[\frac{dV_{C_1}}{dt}\right]_T = -\frac{V_{C_1} - V_{C_d}}{R_d} + (i_{L_1} + i_{L_2})(1 - d_{1or2}) - (i_{L3} + i_{L_4}d_{34}) \tag{45}$$

$$C_2\left[\frac{dV_{out}}{dt}\right]_T = (i_{L_3} + i_{L_4}) - \frac{V_{out}}{R} \tag{46}$$

$$C_d\left[\frac{dV_{C_d}}{dt}\right]_T = \frac{V_{C_1} - V_{C_d}}{R_d} \tag{47}$$

As converter is operating under steady state condition, by applying inductor volt-second law and capacitor charge balance law we can derive following expressions for current and volage.

$$I_g = I_{L_1} + I_{L_2} = \frac{D_{3or4}}{1 - D_{1or2}}\frac{V_{out}}{R} \tag{48}$$

$$I_{out} = I_{L_3} + I_{L_4} = \frac{V_{out}}{R} \tag{49}$$

$$V_{C_1} = \frac{V_s}{1 - D_{1or2}} = \frac{V_{out}}{D_{3or4}} \tag{50}$$

$$V_{C_d} = 0$$

$$V_{out} = D_{3or4}V_{C_1} = \frac{D_{3or4}}{1 - D_{1or2}}V_s \tag{51}$$

Hence, $\frac{V_{out}}{V_s} = \frac{D_{3or4}}{1 - D_{1or2}}$

CIRCUIT DESIGN

Circuit Designing of the converter is based on the motive to reduce pulsating input/output voltage and current ripples. Differential equations obtained by applying the state space averaging techniques on six different modes of operation in the steady-state are used to derive formulas for calculating parameters of different inductors and capacitors in inter leaved buck and boost stage, and analysis of damping circuit for calculating damping capacitor and resist or required in hardware implementation of the proposed converter. Table2 shows formulas for deriving parameters of the components.

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Table2 Formula for deriving parameters of the components.

COMPONENTS	FORMULAS
L_1, L_2	$\frac{V_s(V_{out}-V_s)}{\Delta i_{L_1 or L_2} V_{out}} T$
L_3, L_4	$\frac{V_{out}(V_{out}-V_s)}{\Delta i_{L_3 or L_4} V_{out}} T$
C	$\frac{(V_{out}-V_s)}{\Delta V_{C_1} R} T$
C_o	$\frac{V_{out}(V_{out}-V_s)}{\Delta V_{C_2} R V_s} T$
C_d	>8C
R_d	$0.65\sqrt{\frac{L_{1or2}}{C_1}}$

These formulas are used to derive exact parameters for components, in accordance with experimental proto type. Asper desired ripple current through inductor and ripple voltage across capacitor the values of inductor (L1, L2, L3, and L4) and capacitors (C and Co) are taken. Values of damping circuits capacitor (Cd) and resistor (Rd) can be known now using formulas and values from Table2, and desired output voltage decides the load resistance (RL). Thus, specification for switches (power MOSFETs: M1, M2, M3,and M4) and diodes (D1, D2, D3, and D4) can be known.Table3shows specifications of components used in simulation and hardware. Specifications of components, used to design circuit for simulation and hardware experiment are taken to dc output of 36V, 4.16A, and 150W.

Table3 Specifications of components

COMPONENT	**SPECIFICATIONS**
M1,M2,M3,M	PowerMOSFET:IRF840b
D1,D2,D3,D	SCHOTTKYdiodes:MBR20100
L1,L2	80µH,5A
L3,L4	100µH,5A
C	47µF,100V
C0	68µF,100V
C2	470µF,100V
Rd	1Ω, 1W

EXPERIMENTAL RESULT

Simulation of the proposed inter leaved technique based DC-DC converter were done using MATLAB/Simulink. In buck mode, supply dc voltage Vs is 43V and desired dc load voltage is 36V. In this mode D1 and D2 are zero, where as D3 and D4 are 0.834 i.e. M1 and M2 are open circuited. In boost mode, supply dc voltage Vs is 30V and desired DC load voltage is 36V. In this mode D1 and D2 are 0.27, where as D3 and D4 are 1 i.e. M3 and M4 are close circuited [17]. Different wave forms obtained on scopes were studied and analyzed before hardware implementation. Figure 7(a) shows MATLAB/Simulink model of the converter in buck mode, Figure 7(b) shows the PWM for MOSFETs. Figure 8(a) shows MATLAB/Simulink model of

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converter in boost mode, Figure8 (b) shows PWM for MOSFETs.

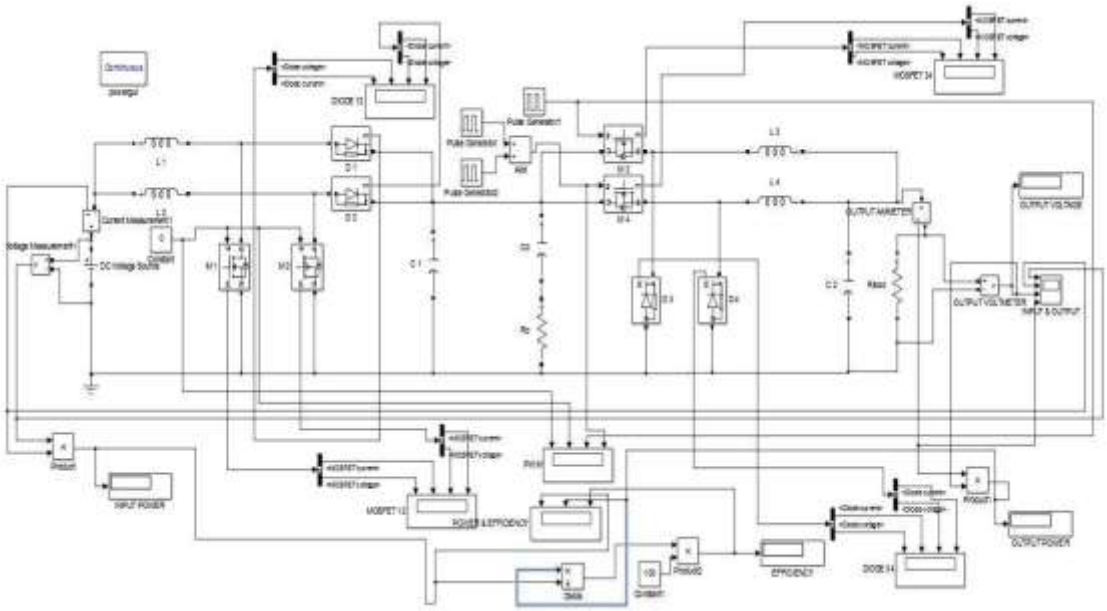
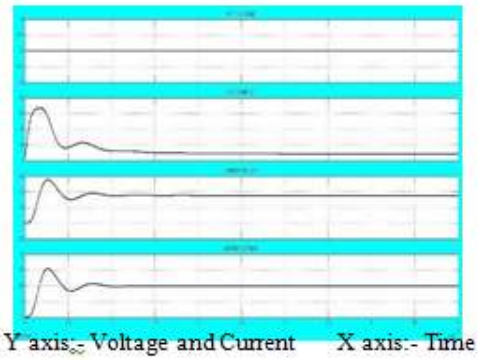


Figure 7(a) MATLAB/Simulink model of converter in buck mode.

Y axis:- Duty Ratio X axis:- Time

Figure 7(b) PWM for MOSFETs in buck mode.



Y axis:- Voltage and Current X axis:- Time

Figure 7(c) voltage and current waveforms in buck mode

Simulation of proposed DC-DC converter verified circuit design, all parameters were studied and satisfied. On basis of the hardware mode l was implemented and tested. Low input/output ripples in voltage and current were observed .Efficiency of converter was more than 90% by calculating the output power ration to the input power ratio with less stress on MOSFETs and diodes.

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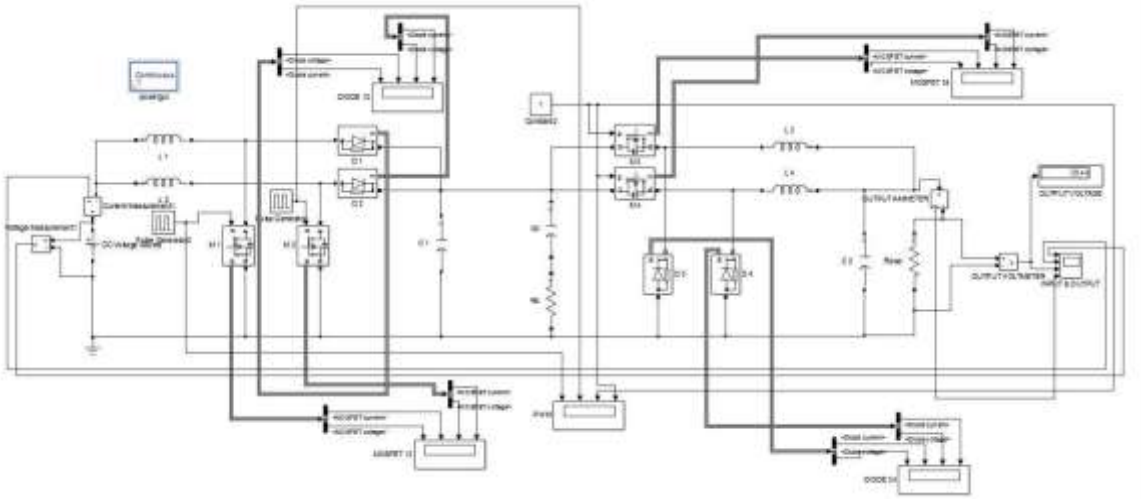

Figure8(a) MATLAB/Simulink model of the converter in boos tmode.

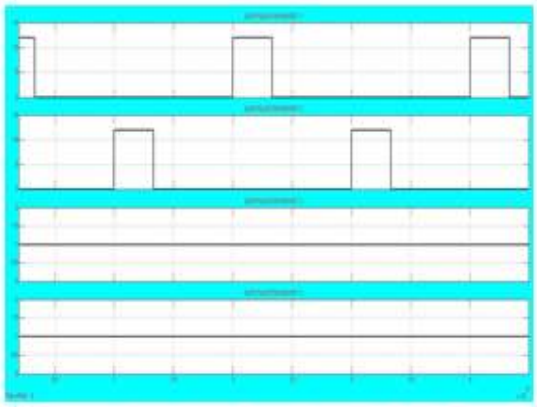

Figure 8(b) PWM for MOSFETs in boost mode.

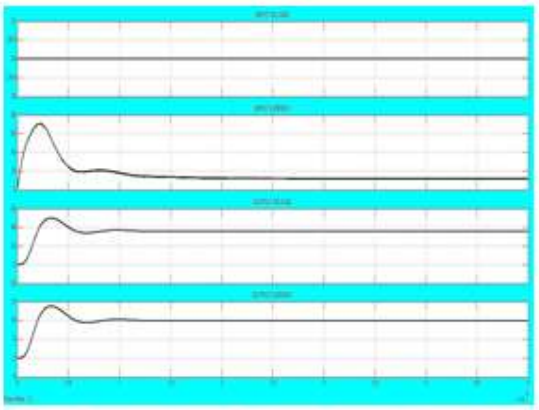

Figure 8(c) voltage and current waveforms in boost mode

Simulation of the proposed DC-DC converter was done to verify all the parameters. On basis of this hardware model was implemented and tested. Low input/output ripples in voltage and current were observed. Efficiency of converter was more than 90% with less stress on MOSFETs and diodes. Figure 9 shows power circuit for proposed converter, and figure 10 shows the controller circuit for proposed converter.

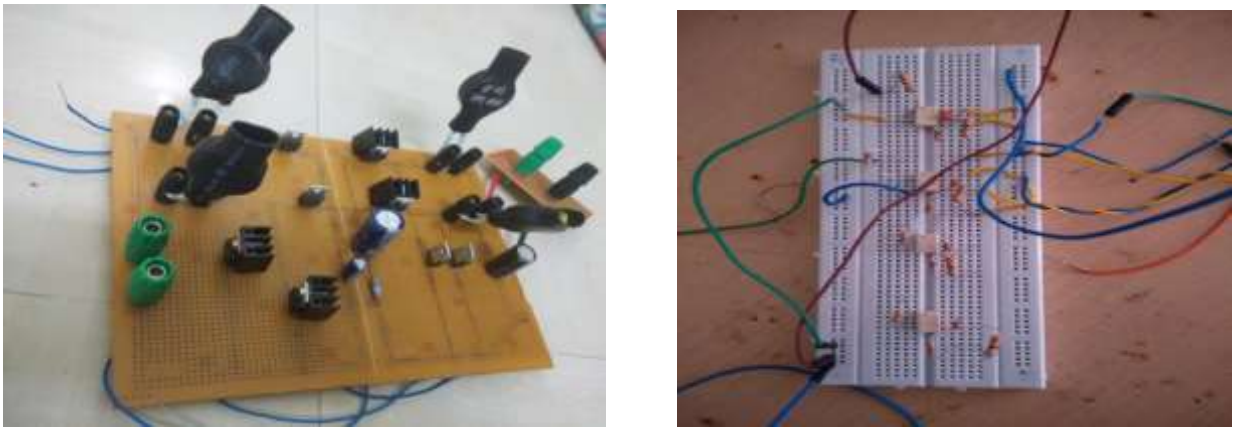

Figure 9 Power circuit and controller circuit for proposed converter

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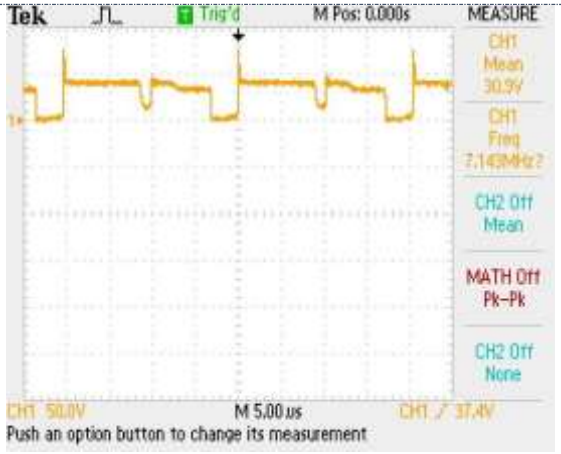
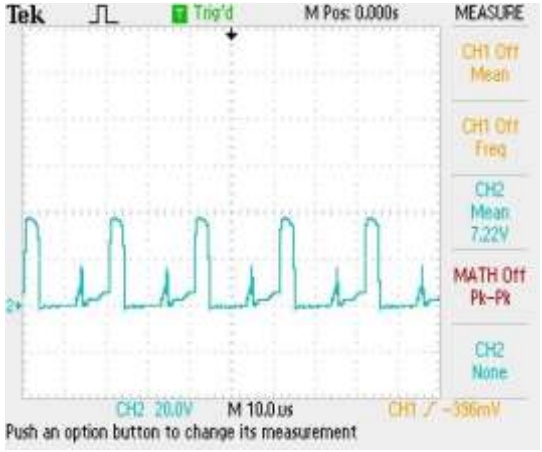
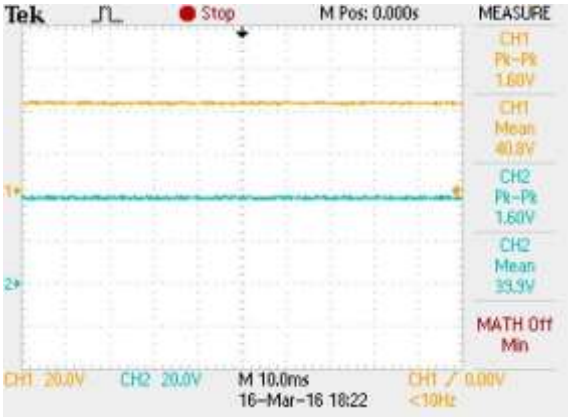


(a) Switch voltage of Boost converter

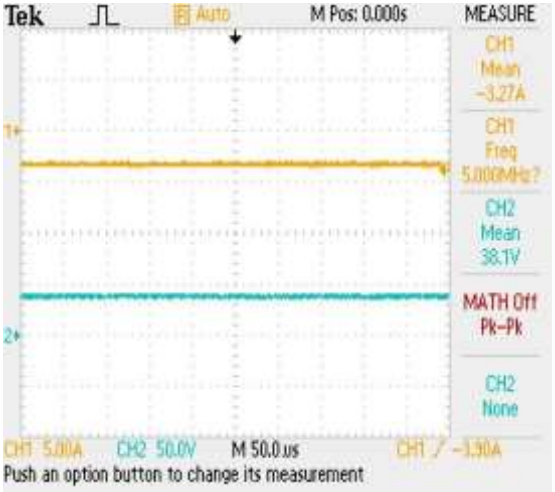
(d) Capacitor and switch voltage of Buck Converter



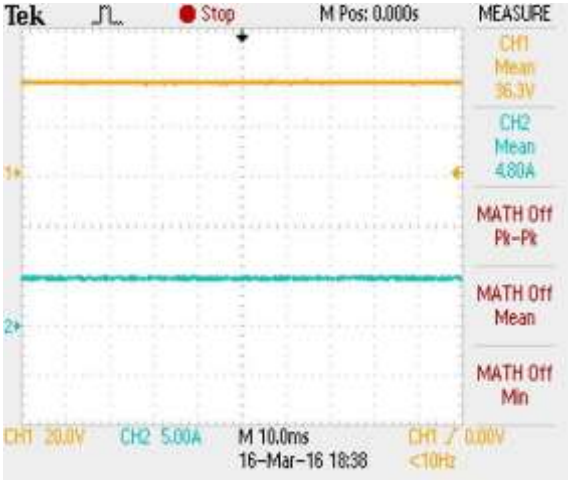
(b)Diode Voltage of Boost Converter



(e) Diode and Capacitor Voltage of Buck Converter



(c) Output Current and Output Voltage Of Boost Converter Converter



(f) Output Voltage and Output Current of Buck

Figure11(a) ,(b) ,(c):experimental results in boost mode;

Figure11 (d) (e) (f):experimental results in buck mode.

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Figure 11 shows the experimental results of the proposed inter leaved technique based buck-boost dc-dc converter. Desired stress on switches and diodes are observed with less voltage and current ripples. Efficiency of the converter was found to be more than 90% with voltage ripple less than 0.2V and current ripple less than 0.1A. The dynamics of the converter was observed high under steady-state of operation.

CONCLUSION

A new buck-boost DC-DC converter based on inter leaved technique was proposed and simulated. The simulation and hardware implementation of the dc-dc converter assured that this dc-dc converter has the ability to reduce voltage oscillations, input/output current ripples, switching stresses and increases dynamics and efficiency. This feature of the proposed converter is useful in many applications such as battery charging, fuel cell, HEV/EV, photo voltaic panels and more. Maximum efficiency in buck or boost mode was obtained by short circuiting or open circuiting two MOSFETs of either buck or boost converter.

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